What is claimed is:

1. A clock generator comprising:

a clock generating circuit having a function for varying a clock phase in accordance with a control signal;

a phase difference detection circuit comparing the clock phase output from said clock generating circuit with a phase of a reference waveform, and detecting a phase difference therebetween; and

a control signal generating circuit generating a control signal for controlling the clock phase of said clock generating circuit, based on phase difference information obtained from said phase difference detection circuit, wherein:

said phase difference detection circuit comprises a plurality of phase detection units;

at least one of said plurality of phase detection units carries out a direct phase detection in which a phase of the clock is directly compared with the phase of the reference waveform; and

at least the other one of said plurality of phase detection units carries out an indirect phase detection using a phase-synchronized waveform generating circuit generating a waveform synchronized in phase with the reference waveform or an output of said clock generating circuit and a phase information extracting circuit extracting phase information from the phase-synchronized waveform.

2. The clock generator as claimed in claim 1, wherein:

in the direct phase detection, the phase of the clock is compared with the phase of the reference waveform at a first frequency; and

in the indirect phase detection, the phase of the clock is compared with the output of said phase-synchronized waveform generating circuit at a second frequency higher than the first frequency.

3. The clock generator as claimed in claim 2, wherein:

the direct phase detection is carried out by detecting a phase difference between the clock and externally supplied data; and

the indirect phase detection is carried out by detecting a phase difference between the clock and a data clock synchronized to the externally supplied data.

4. The clock generator as claimed in claim 3, further comprising:

a clock phase adjusting circuit adjusting the phase of the clock in accordance with a signal generated by said plurality of phase detection units, and wherein a response speed characteristic that affects the phase of the clock is different for each output of said plurality of phase detection units.

5. The clock generator as claimed in claim 4, wherein:

data are transmitted on a plurality of data lines for one data clock line on which the data clock is transmitted;

said data clock line and said data lines are each provided with a clock generating circuit;

said clock generating circuit provided on said data clock line detects a phase difference between the clock generated by said clock generating circuit and the data clock, adjusts the phase of the clock based on a value of the detected phase difference, supplies the control signal used for adjusting the phase to said clock generating circuit provided on each of said data lines, and generates a clock control signal based on the supplied control signal and on a signal representing the phase difference between the clock and the data on said data line.

6. The clock generator as claimed in claim 5, wherein a value corresponding to a rate of increase in

the phase of the data clock is obtained based on phase information obtained from said phase detection unit associated with said data clock line, and is supplied to said clock phase adjusting circuit on said each data line where the clock phase is adjusted based on information concerning the value and on information concerning the phase difference between the clock and the data on said data line.

7. The clock generator as claimed in claim 1, wherein detection of the clock phase is carried out by using:

the phase difference detection circuit comparing an external reference clock with the clock generated by said clock generating circuit, and detecting a phase difference therebetween; and

a phase detection circuit detecting a phase of a PLL or DLL when the clock output from said clock generating circuit is supplied to said PLL or DLL.

8. The clock generator as claimed in claim 7, wherein a value obtained from a phase comparison between the external reference clock and the clock output from said clock generating circuit controls the phase of said clock generating circuit with a long time constant, and phase information obtained from said phase detection circuit of said PLL or DLL controls the phase of said clock generating circuit with a shorter time constant.

9. A clock generator comprising:

a first phase comparator carrying out a phase comparison between an externally supplied reference signal and an internal clock;

a phase-synchronized clock generating circuit generating a comparison clock synchronized in phase to the reference signal and having a higher clock transition rate than the reference signal;

a second phase comparator carrying out a phase comparison between the comparison clock and the internal clock;

an adder summing first phase difference information obtained from said first phase comparator and second phase difference information obtained from said second phase comparator; and

an internal clock generating circuit generating the internal clock whose phase is adjusted in accordance with an output of said adder.

10. The clock generator as claimed in claim 9, further comprising:

a low-pass filter allowing low frequencies contained in an output of said first phase comparator to be transmitted therethrough and supplied to said adder; and

a high-pass filter allowing high frequencies contained in an output of said second phase comparator to be transmitted therethrough and supplied to said adder.

11. The clock generator as claimed in claim 9, wherein the reference signal is an externally supplied reference clock, and the internal clock is generated by multiplying the reference clock.

12. The clock generator as claimed in claim 11, wherein the phase-synchronized clock generating circuit is a multiplying circuit.

13. The clock generator as claimed in claim 9, wherein the reference signal is externally supplied data, and the internal clock is a clock for receiving the data.

14. The clock generator as claimed in claim 9, wherein:

the reference clock is a data clock transmitted on one data clock line with respect to data transmitted in parallel on a plurality of data lines;

the internal clock is generated as a plurality of data receiving clocks for receiving the respective data transmitted on said plurality of data lines;

said second phase comparator is provided

for said data clock line;

said first phase comparator, said adder, and said internal clock generating circuit are provided for each of said plurality of data lines;

each of said adders sums the first phase difference information obtained from said first phase comparator associated therewith and the second phase difference information obtained from said second phase comparator; and

each of said internal clock generating circuits generates the internal clock whose phase is adjusted in accordance with an output of said adder associated therewith.